AMENDMENT TO THE SPECIFICATION

Please replace the paragraph beginning on page 11, line 15, with the following amended paragraph:

By way of example, a frequency synthesizer 156 provides the CLK_{OUT} signal based on the input clock signal CLK_{IN} having a desired maximum frequency (F_{MAX}) and based on an UP/DN control signal. The maximum frequency F_{MAX} is a fixed frequency according to application requirements for the system 150 and the associated ICs implementing the system. The CLK_{IN} signal, for example, is provided (*e.g.*, by a phase locked loop) based on a system clock signal according to customer specifications. Alternatively, the CLK_{IN} signal can be provided by a ring oscillator tuned to F_{MAX}. For example, as shown and described herein, the frequency of the CLK_{OUT} signal can also vary based on V_{SUPPLY}, illustrated schematically at 170. The frequency synthesizer 156 implements adjustments on the CLK_{IN} signal based on the UP/DN control signal, such as provided by frequency control circuitry (not shown). That is, the frequency synthesizer 156 thus provides the CLK_{OUT} signal to have a variable frequency that can be incrementally adjusted based on the UP/DN control signal.